REMARKS

The present response is to the Office Action mailed in the above-referenced case on Sept. 17, 2003. Claims 1-6 are standing for examination. The Examiner has objected to the specification, indicating that the title of the invention is not descriptive, and that the status of the application on page one of the specification requires update. In response, applicant herein amends the title of the invention, and has reviewed the status of the priority applications. As there has been no change in the status of the priority applications, no amendment is made in the paragraph.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Quattromani et al. (U.S. 5,471,590), hereinafter Quattromani. Applicant has carefully studied the prior art presented by the Examiner, and the Examiner's rejections and statements of the instant Office Action. In response, applicant herein presents argument to more particularly point out the subject matter of applicant's invention regarded as patentable, and to establish that the claims, in their present form, distinguish unarguably over the prior art. Applicant points out and argues the key limitations in the base claims that the Examiner appears to have misunderstood in his rejections and statements.

The Examiner has stated that, as per applicant's independent claims 1, 3, and 5, Quattromani teaches all of applicant's claimed limitations, including that write operations that hit in the data cache are stored as elements in the bypass structure before the data is written to the data cache, and read operations use the address matching logic to search the elements of the bypass structure to identify and use any one or more of the entries representing data more recent than that stored in the data cache memory array. Applicant respectfully traverses the

Examiner's above interpretation of Quattromani as anticipating all of applicant's claimed limitations.

Applicant's invention teaches, with reference to Fig. 29, a data cache bypass system 2901 consisting of a six entry bypass structure 2902, and address matching and switching logic 2903, in a unique system allowing continuous execution of loads and stores of arbitrary size to and from the data cache without execution stalls, even in the presence of partial and multiple dependencies between operations executed in different cycles. Each valid entry in the bypass structure represents a write operation which has hit in the data cache but has not yet been written into the actual memory array, and also represents newer data than that in the memory array and are considered logically part of the data cache.

Every read operation utilizes address matching logic (2903) to search all of the entries in the bypass structure to determine if any one or more of the entries represents data more recent than that stored in the data cache memory array. Each memory operation, whether 8-bits, 16-bits or 32-bits in size, is always aligned to the size of the read operation, which may therefore match on multiple entries of the bypass structure and may match only partially with a given entry, meaning that the switching logic which determines where the newest version of a given item of data resides must operate based on bytes. Therefore, a 32-bit read may then get its value from as many as four different locations, some of which are in the bypass structure and some of which are in the data cache memory array itself.

The data cache memory array is dually-ported, and thereby capable of supporting up to two simultaneous operations (read or write) on each bank. Any write can alter data in the data cache memory array without having to read the previous contents of the line in which it belongs. For this reason, a write operation frees up a memory port in the cycle that it is executed and allows a previous write operation, currently stored in the elements of the bypass structure,

to be completed. Given the 32-bit limitation of the memory operations, only a total of six entries are needed at any given time to guarantee that no stalls are inserted and the bypass structure will not overflow.

Quattromani, in contrast, does not specifically teach that the read operations use the address matching logic to search the elements (write operations) of the bypass structure to identify and use any one or more of the entries representing data more recent than that stored in the data cache memory array, such that a subsequent write operation may free a memory port for a write stored in the bypass structure to be written to the data cache memory array, as is taught in applicant's invention and recited in applicant's independent claims.

Quattromani discloses a write buffer located between the microprocessor core and memory, wherein each write to memory executed by the core is made to the write buffer, rather than to the memory bus or data cache, such that cache or memory read operations are not impacted by write operations performed by the microprocessor core. The contents of the write buffer are written into cache or memory in an asynchronous manner in the memory bus or cache becomes available.

It is the Examiner's position that Quattromani specifically teaches that read operations use the address matching logic to search all entries in the write buffer to determine if the entries representing more recent data than that available in the data cache memory array. Applicant, however, respectfully traverses the Examiner position for the following reasons; Quattromani discloses (Col. 21, line 11 to col. 22, line 60), with reference to Fig. 11, a sequence of detecting and handling read after write (RAW) hazards in a microprocessor, wherein in decision 219, write buffer control logic 150 compares the read physical address calculated in process 218 against each of the physical address values in all write buffer entries 152, regardless of pipeline association. The control logic compares the

physical address of the read access to those of the previously allocated addresses, and also considers the span of the operations. In decision 219, if it is determined that there is a match between the physical address calculated for the read operation, and the physical address for one or more write buffer entries 152 that is allocated for an older instruction and has its address valid control bit AV set or that is allocated for a simultaneously allocated write for an older instruction, a read after write (RAW) hazard may exist and the hazard handling sequence illustrated in Fig. 11 continues.

Quattromani, therefore, does not specifically teach or suggest that read operations use the address matching logic to search all entries in the write buffer to determine if the entries representing more recent data than that available in the data cache memory array. Quattromani, in contrast, teaches control logic circuitry coupled to an address calculation stage and to a write buffer, for comparing an address of a read instruction in the calculation stage to the address field of each write buffer entry, and responsive to an address match, the data control bit being set, and non-cacheable write bit being clear, bypassing the data field in the write buffer to the execution stage in the core unit.

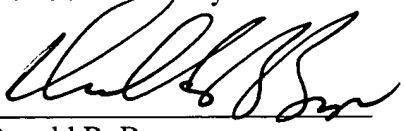
Quattromani clearly teaches an alternative invention for accomplishing an alternative purpose than that of applicant's invention. Quattromani does not utilize the address matching and switching logic for determining if entries in the bypass structure represent newer data than that available in the data cache memory array. The rather common practice of Examiner's in rejecting claims because prior art teaches alternative inventions that might accomplish the same or similar purpose is not provide prima facie rejections, and should be discouraged. An invention by another that solves a similar problem that applicant's invention solves, does not necessarily anticipate applicant's invention. To create a prima

facie rejection, the actual elements of the claimed invention must be shown in the art, which is clearly not the case in this instance.

Applicant's independent claims 1, 3 and 5 each recite searching the bypass structure entries by the read operations, and address matching and switching logic which searches all entries in the bypass structure and determines if any of the entries represent newer data than that available in the data cache memory array, which Quattromani clearly does not specifically teach, suggest or intimate. Applicant therefore strongly believes that the independent claims are clearly and unarguably patentable over Quattromani. Depending claims 2, 4 and 6 are then patentable on their own merits, or at least as depended from a patentable claim.

It is therefore respectfully requested that this application be reconsidered, the claims be allowed, and that this case be passed quickly to issue. If there are any time extensions needed beyond any extension specifically requested with this amendment, such extension of time is hereby requested. If there are any fees due beyond any fees paid with this amendment, authorization is given to deduct such fees from deposit account 50-0534.

Respectfully Submitted,
Mario Nemirovsky et al.

by 

Donald R. Boys
Reg. No. 35,074

Donald R. Boys
Central Coast Patent Agency
P.O. Box 187
Aromas, CA 95004
(831) 726-1457